



S/N 10/783,695

**PATENT****IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Leonard Forbes  
Serial No.: 10/783,695  
Filed: February 20, 2004  
Title: DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS

Examiner: Bradley Smith  
Group Art Unit: 2891  
Docket: 1303.019US2

**COMMUNICATION CONCERNING RELATED APPLICATIONS**

MS RCE  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Applicant would like to bring to the Examiner's attention the following related applications in the above-identified patent application:

| <u>Serial/Patent No.</u> | <u>Filing Date/Issue Date</u> | <u>Attorney Docket</u> | <u>Title</u>   |
|--------------------------|-------------------------------|------------------------|--|
| 11/202460                | August 12, 2005               | 1303.027US3            | SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS |
| 11/212190                | August 26, 2005               | 1303.024US3            | INTEGRATED CIRCUIT MEMORY DEVICE AND METHOD                                    |

Continuations and divisionals may be later filed on the cases listed above, or cited to the Examiner in any previous Communication Concerning Related Applications. Applicants request that the Examiner review all continuations and divisionals of the above-listed or previously-cited patent applications before allowing the claims of the present patent application.

Respectfully submitted,

LEONARD FORBES

By Applicant's Representatives,

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Date 17 MARCH 2006 By David R. Cochran  
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**CERTIFICATE UNDER 37 CFR 1.8:** The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 17 day of March, 2006.

LISA ROSORSKE  
Name

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Signature